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LOGIC DESIGN LAB (10ESL38) ... Aim: (i) Realization of parallel adder/Subtractors using 7483 chip ... LD LAB Manual (Repaired) Author:

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<http://elearning.vtu.ac.in/15/E-Notes/Logicdeslab/LD%20Manual.pdf>

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Digital Electronics Lab SSIT 10 Experiment No: Date: __/__/____ PARALLEL ADDER AND SUBTRACTOR USING 7483 Aim: - To realize IC7483 as parallel adder / Subtractor.

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<http://info2myfriends.blog.com/files/2010/11/Digital-Electronics-labmanual.doc>

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http://ggnindia.dronacharya.info/CSEDept/Downloads/Labmanuals/Aug09-Dec09/CSE%20&%20IT/III%20sem/LM_Digital_Electronics_SemIII.pdf

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DIGITAL ELECTRONICS - uCoz

http://ecalpha.ucoz.com/S5-IC-LAB/digital_lab_manual_final.doc

Study the laboratory instruction manual thoroughly prior to each lab ... numbers using parallel adders. The adder/subtractor ...
3 adder circuit using 7483 ...

Experiment No 1 - India Study Channel - IndiaStudyChannel ...

<http://www.indiastudychannel.com/attachments/Resources/127861-25543-LOGIC-DESIGN-LAB-MANUAL.doc>

... REALISATION of parallel adder/subtractor using 7483 Chip ... REALISATION of Parallel adder/subtractor using 7483chip
(2) BCD to XS3 code conversion and vice versa.

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